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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,365	09/14/2004	Anthony G. Domenicucci	18034	5364

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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,365	DOMENICUCCI ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-19 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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Claim Rejections

Set of claims 1-14

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9-10 and 12-14 are rejected under 35 USC 102 (b) as being anticipated by Cabral, JR. et al.

Cabral, JR. et al. teach a method of forming a metal silicide 12 on a surface of a Si-containing material 10 (figs. 1A-1G and related texts) comprising the steps of:

providing a structure comprising a metal-containing silicon alloy layer 12 (col 4, line 11 and 18) over a Si-containing material;

subjecting said structure to a first anneal (figs. 1b - 1d and col 4, line 60, col 5, line 5) which comprises a first thermal cycle which is performed at a first temperature (fig. 1c and col 4, line 60) that enhances uni-directional diffusion of said metal into said Si-containing material thereby forming an amorphous metal-containing silicide 16 and a second thermal cycle which is performed at a second temperature (col 4, line 5) that converts the amorphous metal-containing silicide into a crystallized metal rich silicide 18 that is substantially non-etchable (col 5, lines 9,21,35,50) as compared to the metal-

containing silicon alloy layer; removing any unreacted metal-containing silicon alloy layer from the structure; and

subjecting said structure to a second anneal at a third temperature (col 5, lines 45-67) that converts said crystallized metal rich silicide into a metal silicide phase that is in its lowest resistance phase.

Regarding claim 2, wherein said metal-containing silicon alloy layer 12 is formed by deposition of the alloy layer or by first depositing a refractory metal to form a metal layer and then doping the refractory metal layer with silicon (col 3, lines 60- 67).

Regarding claim 3, further comprising forming an optional barrier layer 14 over said metal-containing silicon alloy layer prior to said first anneal, wherein said optional barrier layer is removed in said removing of the unreacted metal-containing silicon alloy layer 12 (figs. 1d-1e).

Regarding claim 4, wherein said metal-containing silicon alloy layer 12 further comprises at least one additive selected from the group consisting of C, Al, Ge, Sc, Ti, V, Cr, Mn, Fe, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof (col 4, lines 10 and 20).

Regarding claim 5, wherein said metal-containing silicon alloy layer comprises less than about 30 atomic % Si (col 4, lines 10 and 20).

Regarding claim 6, wherein said metal-containing silicon alloy comprises Ni, Co or alloys thereof (col 4, lines 10 and 20).

Regarding claim 7, wherein said first temperature (col 4, line 64) is less than said second temperature (col 5, line 15).

Regarding claim 9, wherein said first thermal cycle is performed for a time period from about 30 seconds to about 120 seconds (col 4, lines 64).

Regarding claim 10, wherein said second temperature is less than about 450°C, yet greater than the first temperature (col 5, line 15).

Regarding claim 12, wherein said second thermal cycle is performed for a time period from about 10 seconds to about 30 seconds. (col 5, line 16).

Regarding claim 13, wherein said removing comprises a wet etch process in which a chemical etchant is employed (col 5,line 30-35).

Regarding claim 14, wherein said third temperature is from about 700°to about 900°C (col 5, line 62) and said second anneal is carried out for a time period from about 300 seconds or less (col 5, line 16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cabral, JR. et al. in view of the following remark.

Regarding claim 8, Cabral, JR. et al. teaches the claimed invention as applied to claim 1 including first temperature is about 350°C- 450°C (col 4, line 64), but fails to teaches first temperature is less than about 350°C as cited in current claim.

However, given the cumulative teaching of Cabral, JR. et al. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for first temperature is less than about 350°C through routine experimentation and optimization to obtain optimal device performance.

Regarding claim 11, Cabral, JR. et al. teaches the claimed invention as applied to claim 1 including second temperature is from about 400°to about 700°C (col 5, line 15), but fails to teaches second temperature is from about 350°to about 400°C as cited in current claim.

However, given the cumulative teaching of Cabral, JR. et al. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for second temperature is from about 350°to about 400°C through routine experimentation and optimization to obtain optimal device performance.

Set of claims 15- 25

Claims 15-19, 22 and 23-25 are rejected under 35 USC 102 (b) as being anticipated by Cabral, JR. et al.

Cabral, JR. et al. teaches a method of forming a cobalt disilicide 12 on a surface of a Si-containing material 10 comprising the steps of:

providing a structure comprising a cobalt (Co) silicon alloy layer 12 over a Si-containing material;

subjecting said structure to a first anneal (col 4, lines 60 and col 5, line 5)which comprises a first thermal cycle (col 4, line 60) which is performed at a first temperature that enhances uni-directional diffusion of Co into said Si-containing material thereby forming an amorphous Co silicide 16 and a second thermal cycle which is performed at a second temperature that converts the amorphous Co silicide into a crystallized Co rich silicide 18 that is substantially non-etchable (col 5, lines 9,21,35,50) as compared to the Co silicon alloy layer

removing any non-reacted Co silicon alloy layer from the structure; and

subjecting said structure to a second anneal at a third temperature (col 5, lines 45-67) that converts said crystallized Co rich silicide into Co disilicide.

Regarding claims 16-19, these claims are rejected under the same rationale set forth above to claims 2- 5.

Regarding claim 22, this claim is rejected under the same rationale set forth above to claim 10.

Regarding claim 24, this claim is rejected under the same rationale set forth above to claim 13

Regarding claim 25, this claim is rejected under the same rationale set forth above to claim 14.

Claims 20- 21 and 23 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cabral, JR. et al. in view of the following remark.

Cabral, JR. et al. teaches the claimed invention as applied to claim 15 including first temperature is about 350°C- 450°C (col 4, line 64), but fails to teaches first temperature is less than about 350°C and from 270°C -352°C as cited in current claims.

However, given the cumulative teaching of Cabral, JR. et al. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for first temperature is less than about 350°C and from 270°C -352°C through routine experimentation and optimization to obtain optimal device performance.

Regarding claim 23, Cabral, JR. et al. teaches the claimed invention as applied to claim 15 including second temperature is from about 400°to about 700°C (col 5, line 15), but fails to teaches second temperature is from about 350°to about 400°C as cited in current claim.

However, given the cumulative teaching of Cabral, JR. et al. It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for second temperature is from about 350°to about 400°C through routine experimentation and optimization to obtain optimal device performance.

Response to Amendment and Argument.

Claims 1 and 15 have been amended,

Claims 8 and 20 have been canceled.

Claims 1-7,9-19 and 21-25 are remained.

Set of claims 1-14

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 7, 9- 14 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cabral, JR. et al. in view of the following remark.

Cabral, JR. et al. teach a method of forming a metal silicide 12 on a surface of a Si-containing material 10 (figs. 1A-1G and related texts) comprising the steps of:

providing a structure comprising a metal-containing silicon alloy layer 12 (col 4, line 11 and 18) over a Si-containing material;

subjecting said structure to a first anneal (figs. 1b - 1d and col 4, line 60, col 5, line 5) which comprises a first thermal cycle which is performed at a first temperature (fig. 1c and col 4, line 60) that enhances uni-directional diffusion of said metal into said Si-containing material thereby forming an amorphous metal-containing silicide 16 and a second thermal cycle which is performed at a second temperature (col 4, line 5) that converts the amorphous metal-containing silicide into a crystallized metal rich silicide 18 that is substantially non-etchable (col 5, lines 9,21,35,50) as compared to the metal-containing silicon alloy layer; removing any unreacted metal-containing silicon alloy layer from the structure; and subjecting said structure to a second anneal at a third temperature (col 5, lines 45- 67) that converts said crystallized metal rich silicide into a metal silicide phase that is in its lowest resistance phase.

Cabral, JR. et al. teach the first temperature of from about 350 C to about 450 C . Cabral, JR. et al does not teach a first temperature of less than about 350 C (fig. 1c and col 4, line 64) as cited in current claim 1.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the workable or optimal ranges for the first temperature of from about 350 C to about 450 C having a modified first temperature of less than about 350 C through routine experimentation and optimization to obtain optimal device performance.In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, wherein said metal-containing silicon alloy layer 12 is formed by deposition of the alloy layer or by first depositing a refractory metal to form a metal layer and then doping the refractory metal layer with silicon (col 3, lines 60- 67).

Regarding claim 3, further comprising forming an optional barrier layer 14 over said metal-containing silicon alloy layer prior to said first anneal, wherein said optional barrier layer is removed in said removing of the unreacted metal-containing silicon alloy layer 12 (figs. 1d-1e).

Regarding claim 4, wherein said metal-containing silicon alloy layer 12 further comprises at least one additive selected from the group consisting of C, Al, Ge, Sc, Ti, V, Cr, Mn, Fe, Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof (col 4, lines 10 and 20).

Regarding claim 5, wherein said metal-containing silicon alloy layer comprises less than about 30 atomic % Si (col 4, lines 10 and 20).

Regarding claim 6, wherein said metal-containing silicon alloy comprises Ni, Co or alloys thereof (col 4, lines 10 and 20).

Regarding claim 7, wherein said first temperature (col 4, line 64) is less than said second temperature (col 5, line 15).

Regarding claim 9, wherein said first thermal cycle is performed for a time period from about 30 seconds to about 120 seconds (col 4, lines 64).

Regarding claim 10, wherein said second temperature is less than about 450°C, yet greater than the first temperature (col 5, line 15).

Regarding claim 11, Cabral, JR. et al. teaches the claimed invention as applied to claim 1 including second temperature is from about 400° to about 700°C (col 5, line 15), but fails to teaches second temperature is from about 350°to about 400°C as cited in current claim.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the workable or optimal ranges for the second temperature is from about 400° to about 700°C having a modified second temperature is from about 350°to about 400°C through routine experimentation and optimization to obtain optimal device performance.In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 12, wherein said second thermal cycle is performed for a time period from about 10 seconds to about 30 seconds. (col 5, line 16).

Regarding claim 13, wherein said removing comprises a wet etch process in which a chemical etchant is employed (col 5,line 30-35).

Regarding claim 14, wherein said third temperature is from about 700°to about 900°C (col 5, line 62) and said second anneal is carried out for a time period from about 300 seconds or less (col 5, line 16).

Set of claims 15- 25

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cabral, JR. et al. in view of the following remark.

Cabral, JR. et al. teaches a method of forming a cobalt disilicide 12 on a surface of a Si-containing material 10 comprising the steps of:

providing a structure comprising a cobalt (Co) silicon alloy layer 12 over a Si-containing material;

subjecting said structure to a first anneal (col 4, lines 60 and col 5, line 5)which comprises a first thermal cycle (col 4, line 60) which is performed at a first temperature that enhances uni-directional diffusion of Co into said Si-containing material thereby forming an amorphous Co silicide 16 and a second thermal cycle which is performed at a second temperature that converts the amorphous Co silicide into a crystallized Co rich silicide 18 that is substantially non-etchable (col 5, lines 9,21,35,50) as compared to the Co silicon alloy layer removing any non-reacted Co silicon alloy layer from the structure;

and subjecting said structure to a second anneal at a third temperature (col 5, lines 45-67) that converts said crystallized Co rich silicide into Co disilicide.

Cabral, JR. et al. does not teach first temperature is about 350°C- 450°C (col 4, line 64), but does no teach first temperature is less then 350°C.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the workable or optimal ranges for the first temperature of from about 350 C to about 450 C having a modified first temperature of less than about 350 C through routine experimentation and optimization to obtain optimal device performance.In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 16-19, these claims are rejected under the same rationale set forth above to claims 2- 5.

Regarding claim 22, this claim is rejected under the same rationale set forth above to claim 10.

Claims 21 and 23 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Cabral, JR. et al. in view of the following remark.

Cabral, JR. et al. teaches the claimed invention as applied to claim 15 including first temperature is about 350°C- 450°C (col 4, line 64), but fails to teaches first temperature is from 270°C -352°C as cited in current claims.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the workable or optimal ranges for the first temperature of

from about 350 C to about 450 C having a modified first temperature is from 270°C - 352°C through routine experimentation and optimization to obtain optimal device performance.In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 23, Cabral, JR. et al. teaches the claimed invention as applied to claim 15 including second temperature is from about 400°to about 700°C (col 5, line 15), but fails to teaches second temperature is from about 350°to about 400°C as cited in current claim.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the workable or optimal ranges for the first temperature of from about 350 C to about 450 C having a modified second temperature is from about 400°to about 700°C through routine experimentation and optimization to obtain optimal device performance.In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 24, this claim is rejected under the same rationale set forth above to claim 13

Regarding claim 25, this claim is rejected under the same rationale set forth above to claim 14.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, M.Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818